

# PG161-A00

TU106 6GB GDDR6, 192b, X16  
DVI-D/DP + DP + HDMI

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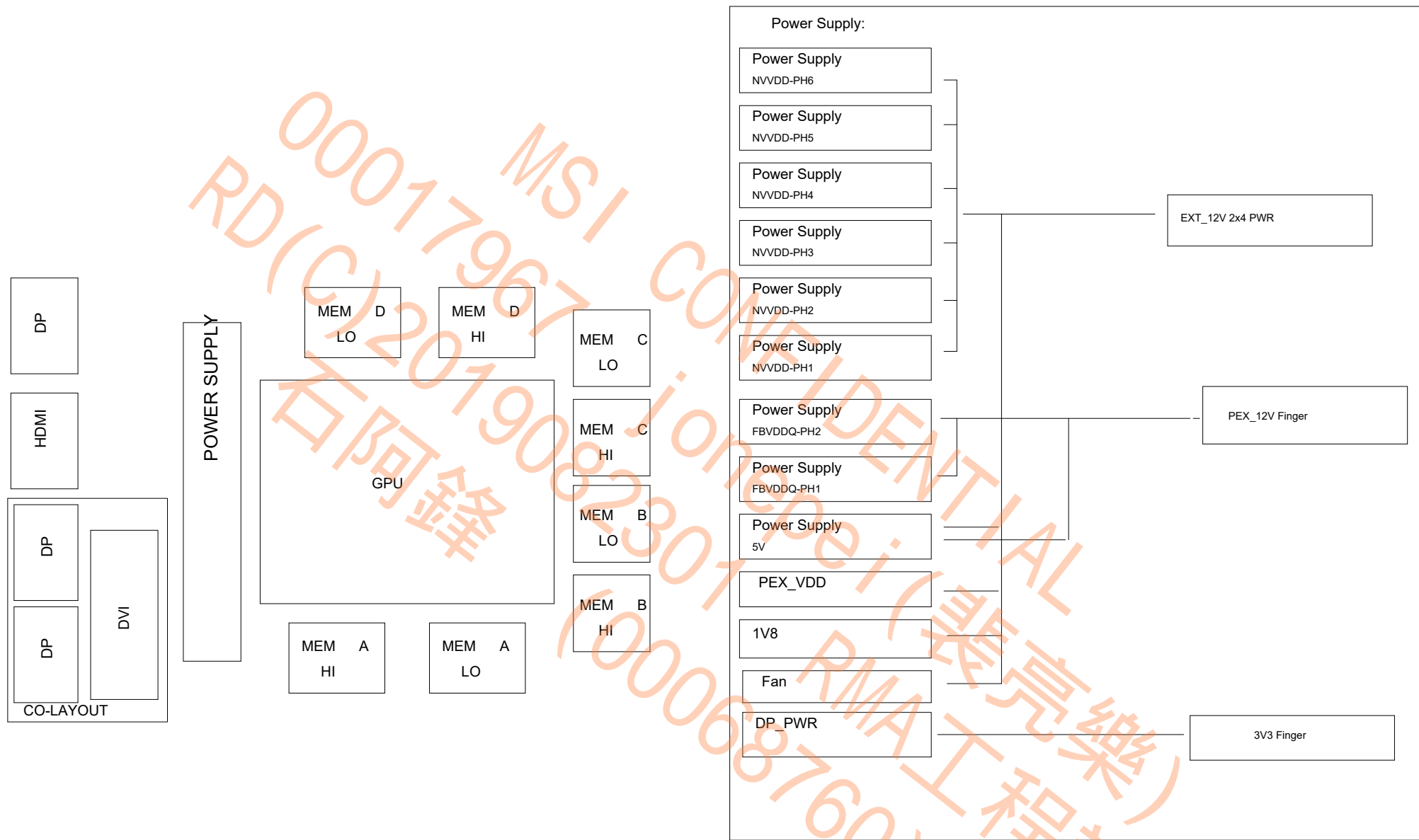
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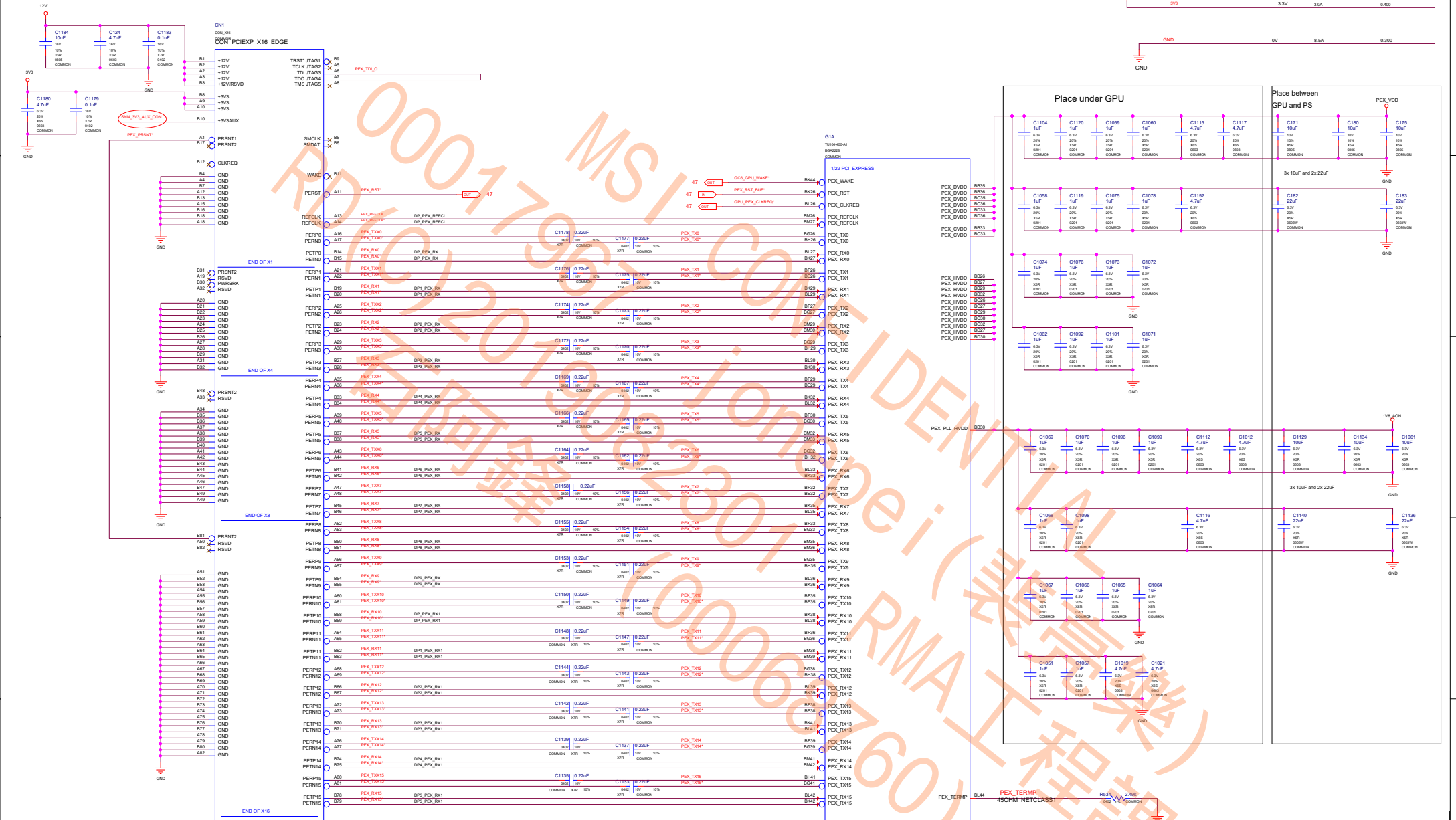
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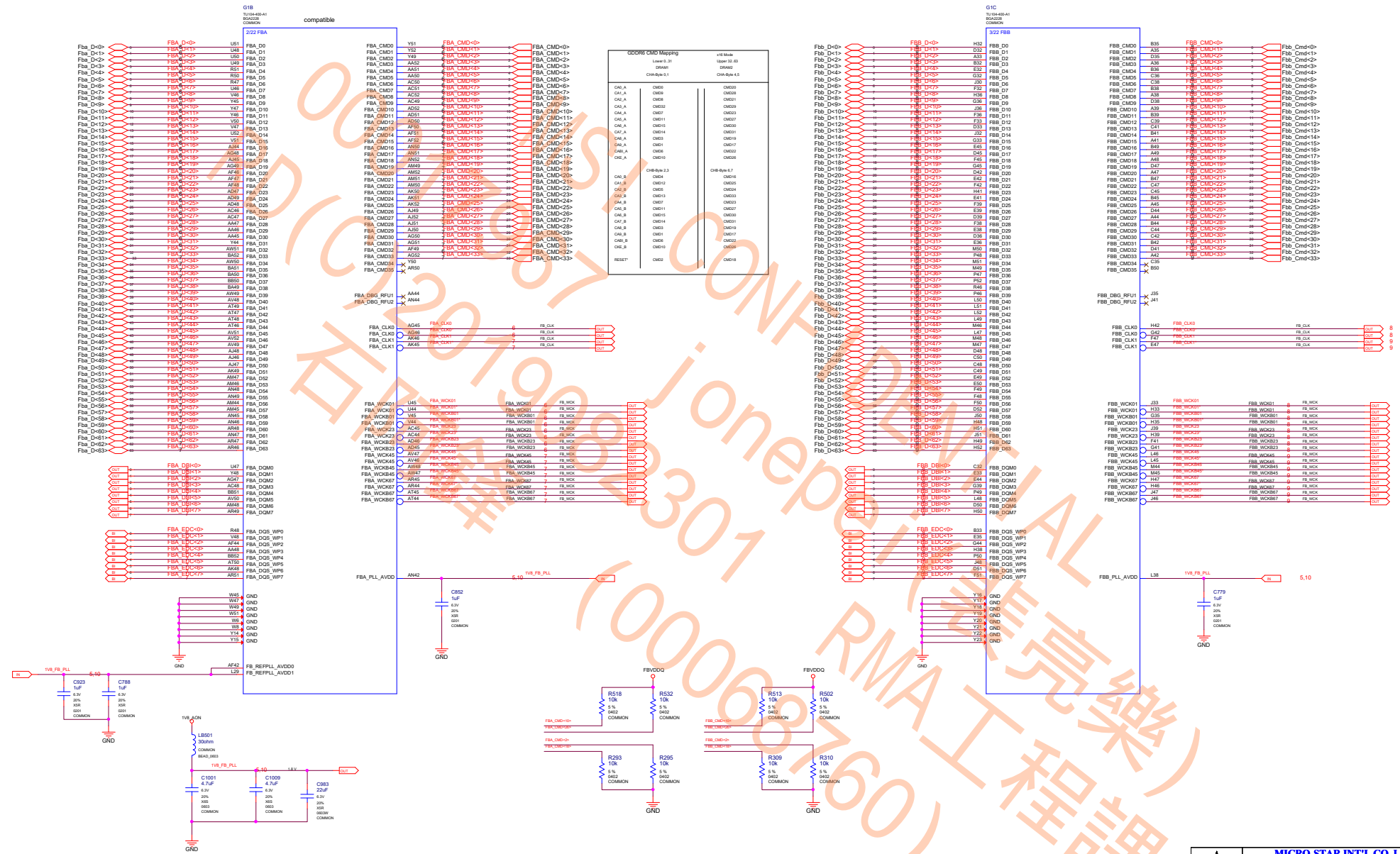
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NO PEX GEN4 SUPPORT  
DELETE RC TERMINATIONS

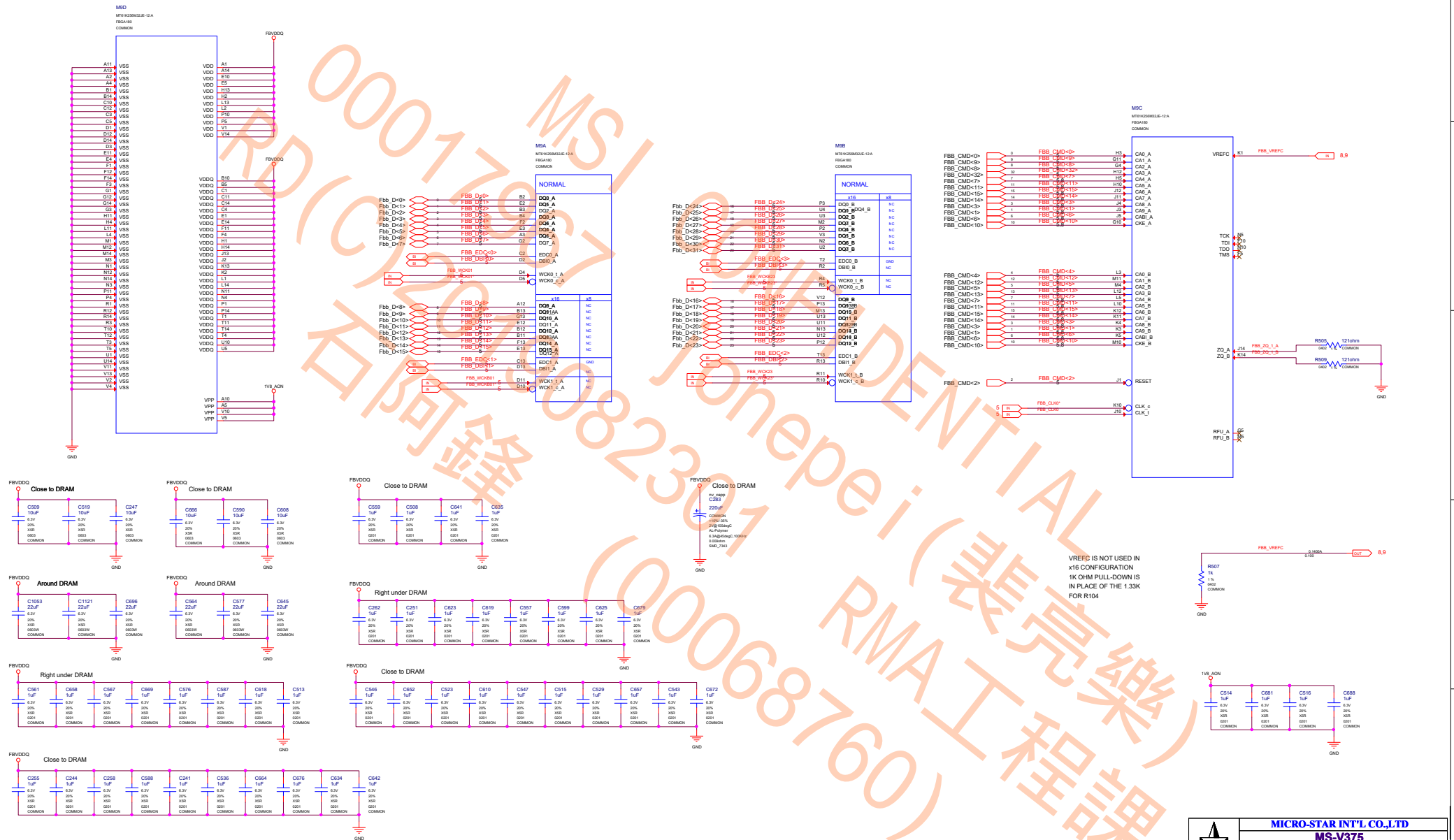
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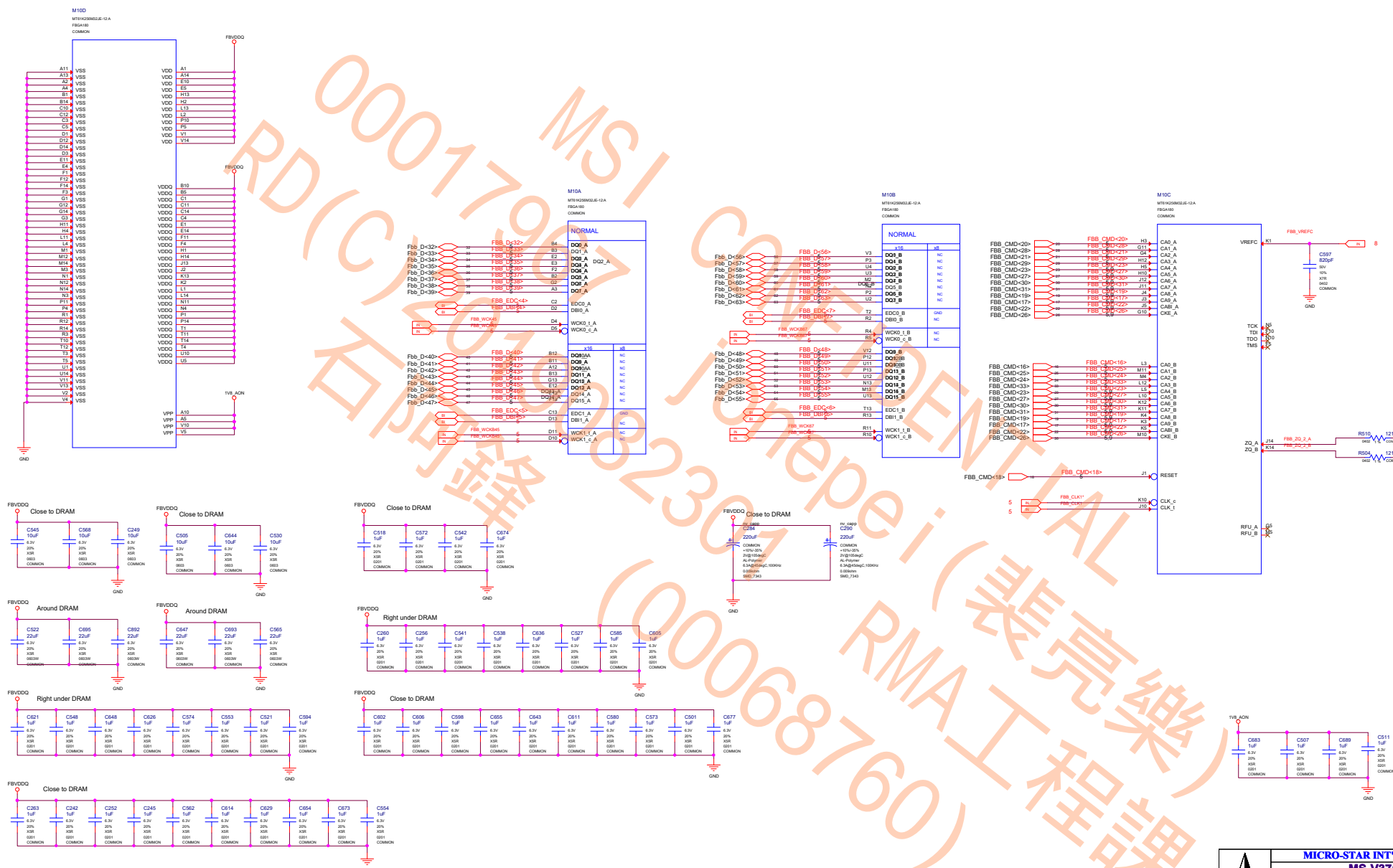


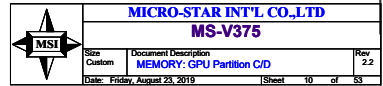


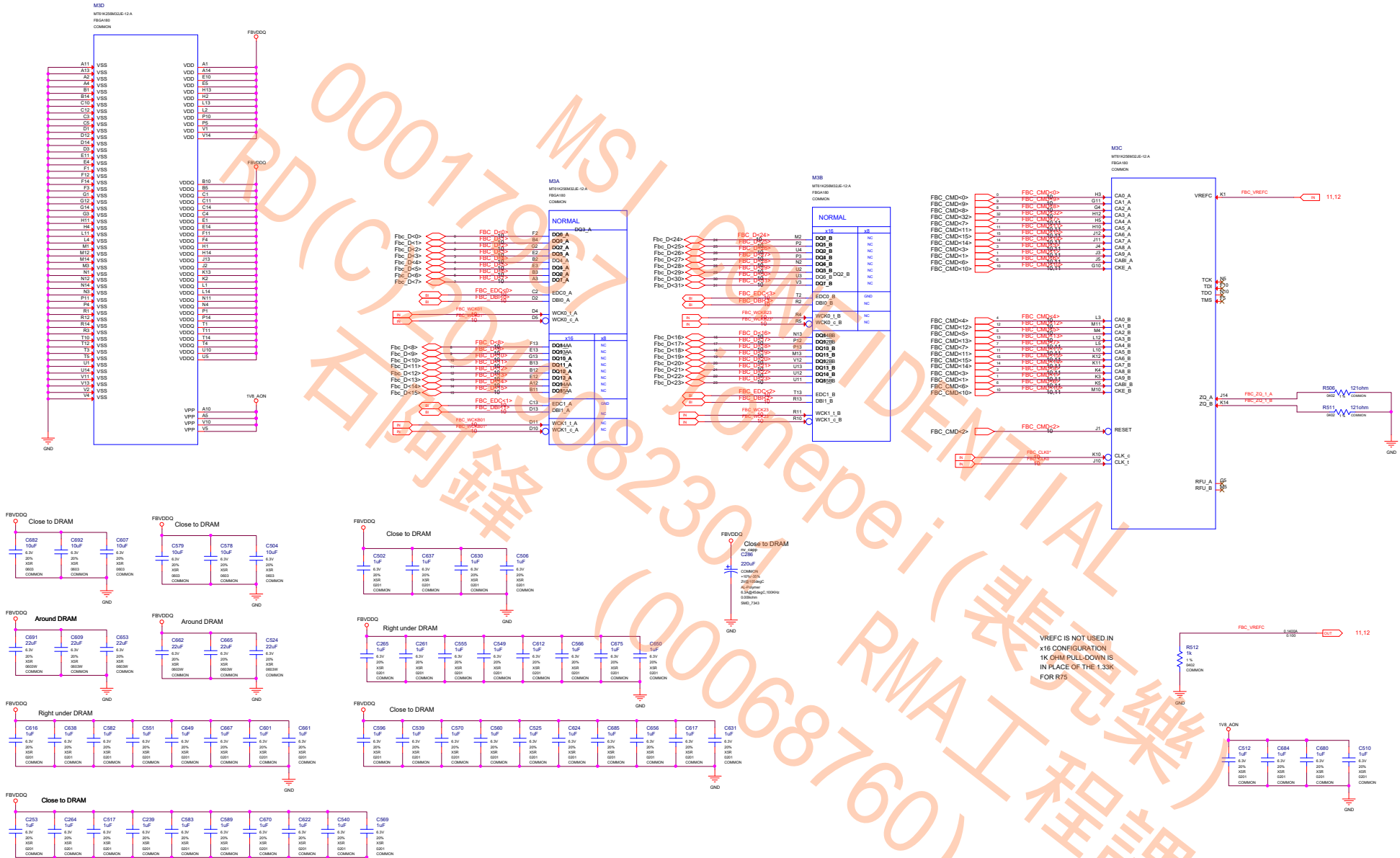


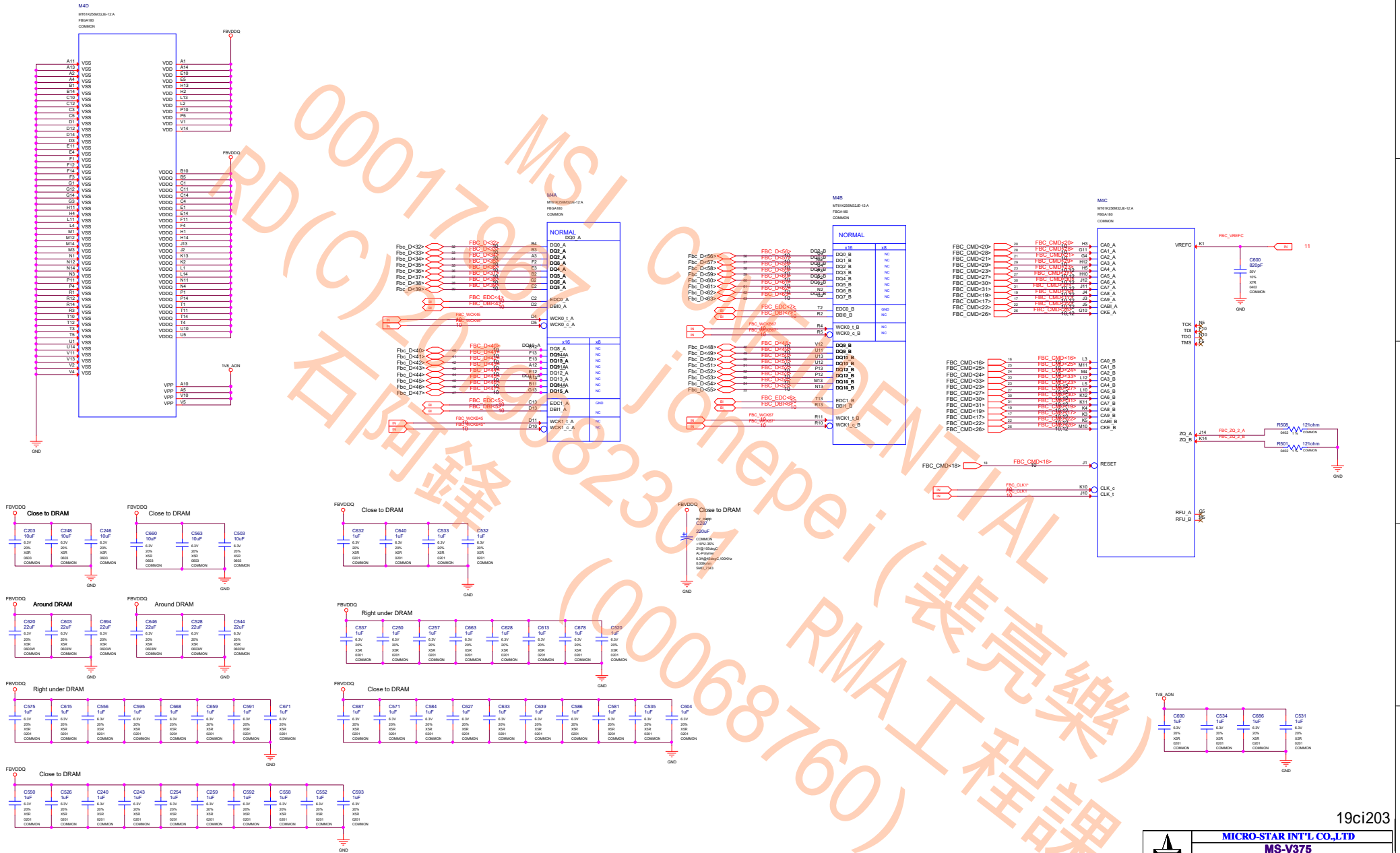


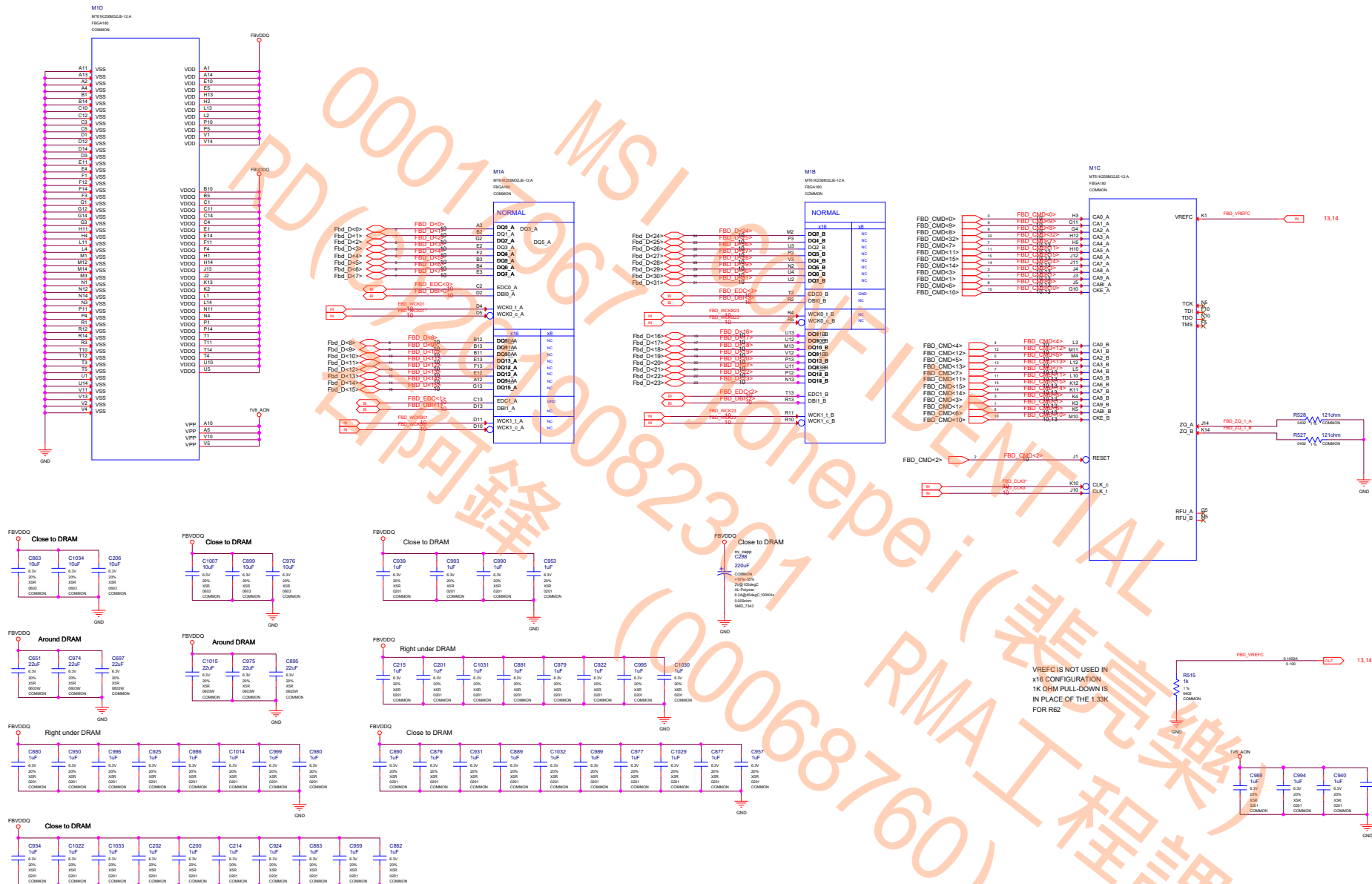


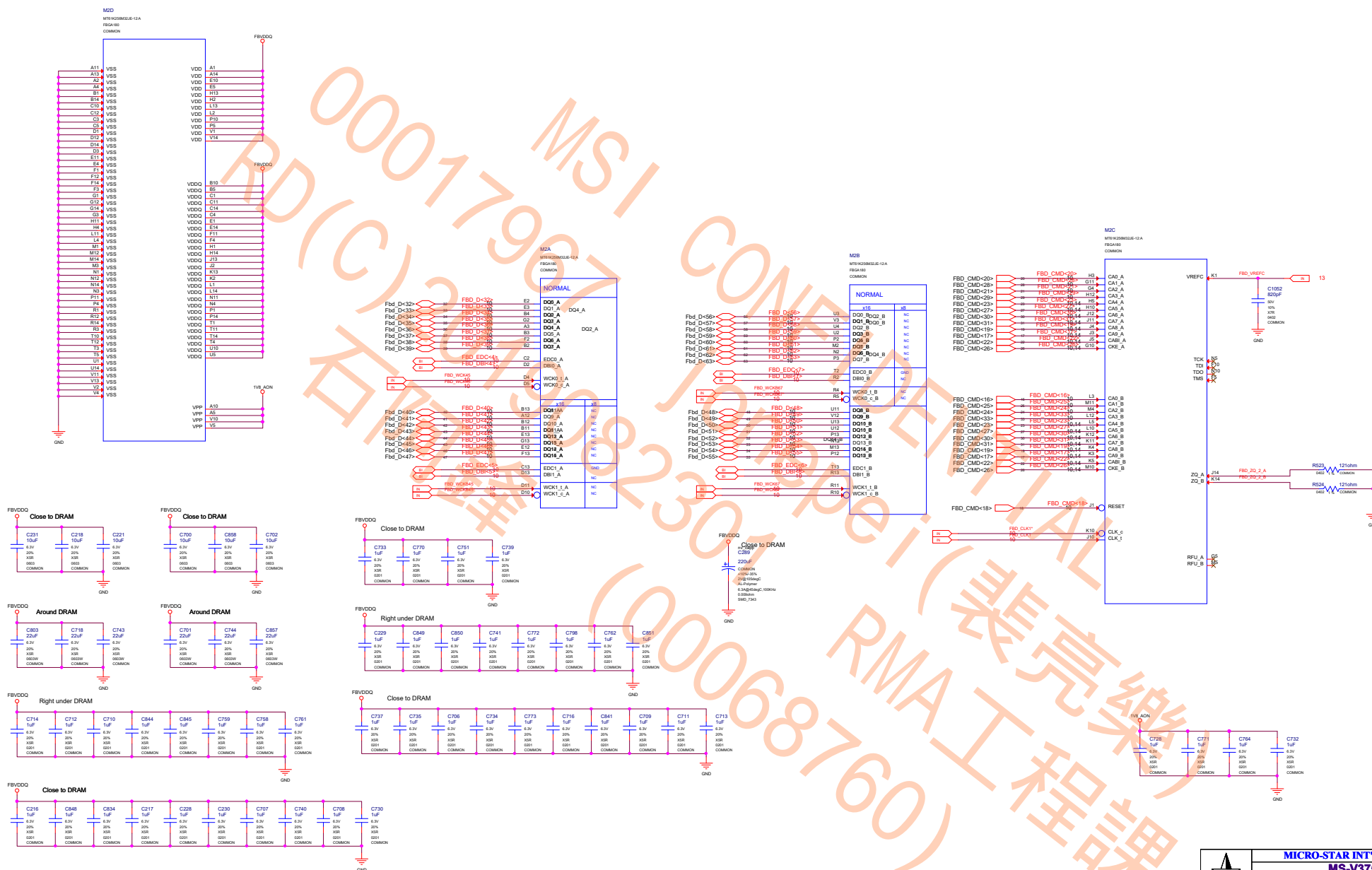














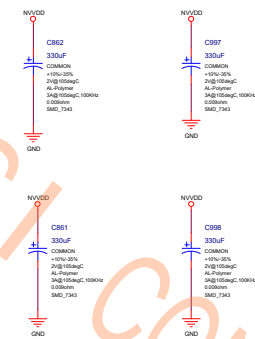




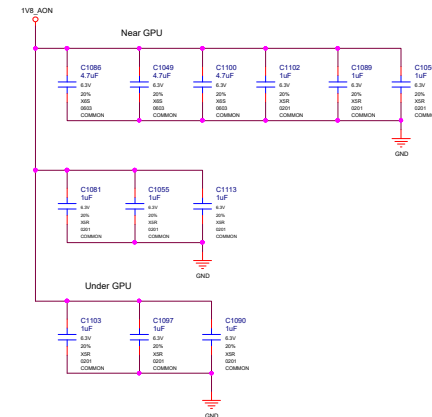
## FBVDDQ



## NVVDD



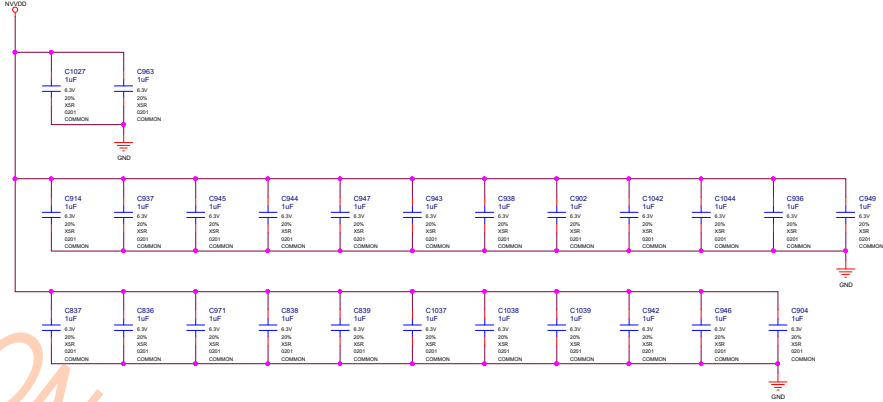
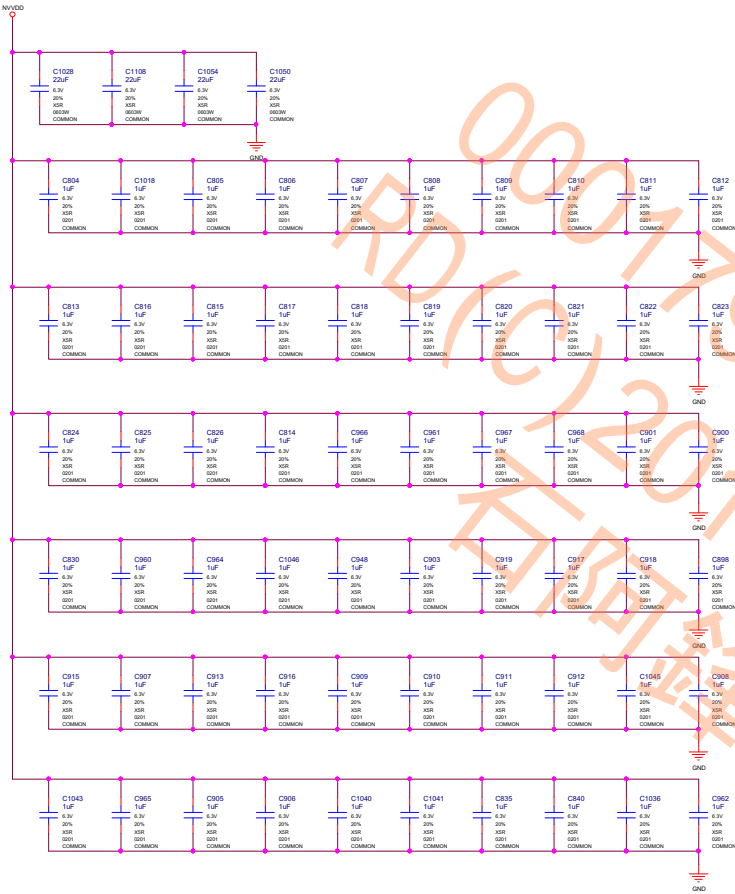
## 1V8\_AON



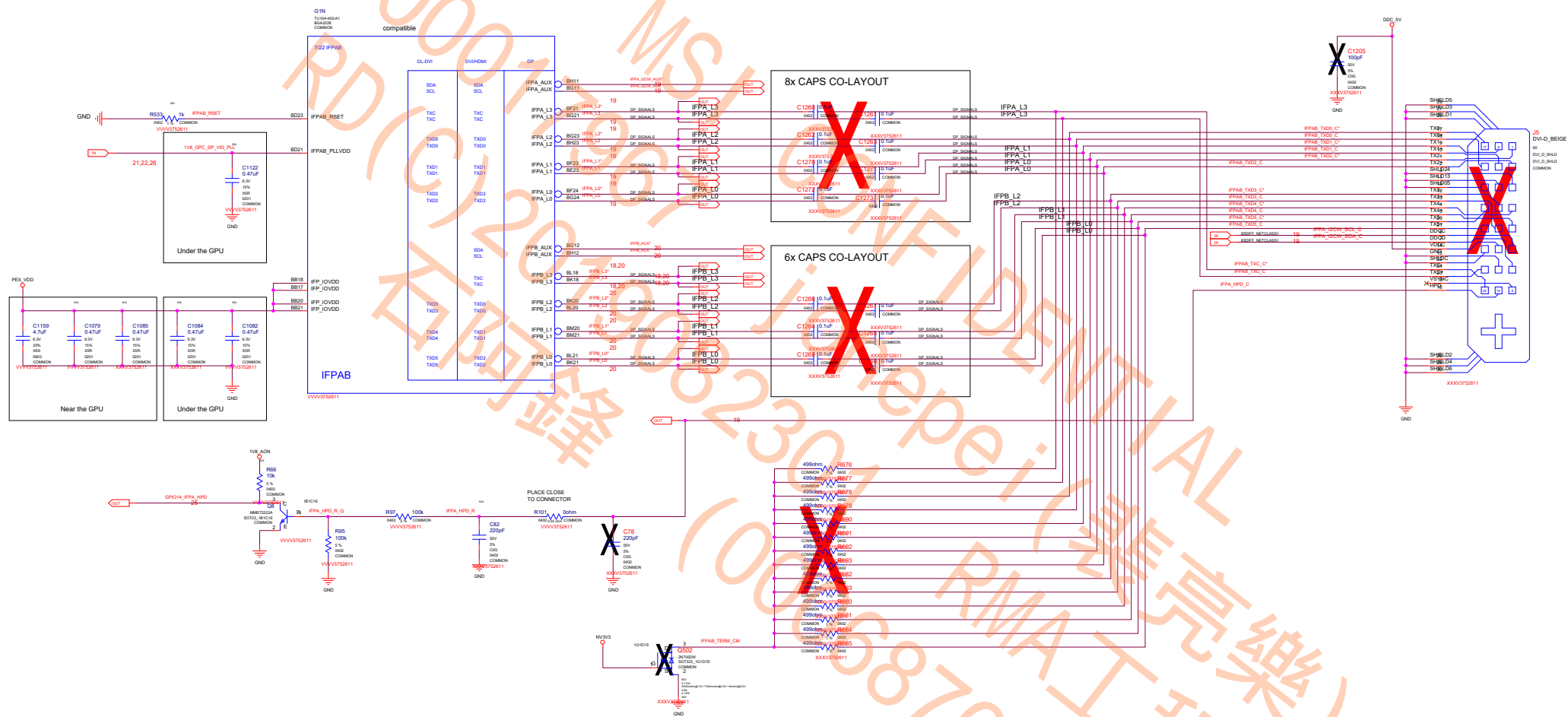
19ci203

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NVDD

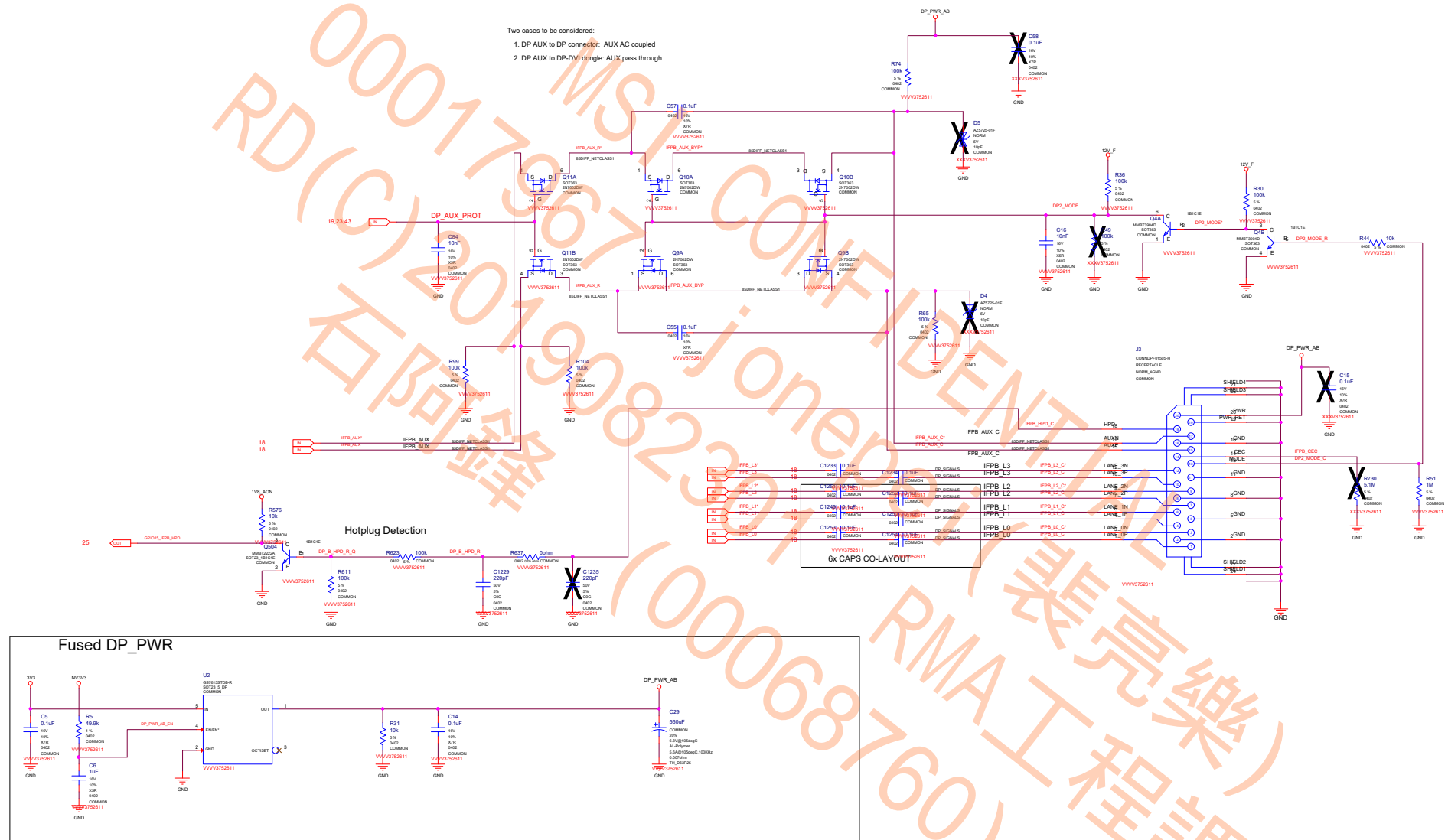


# IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



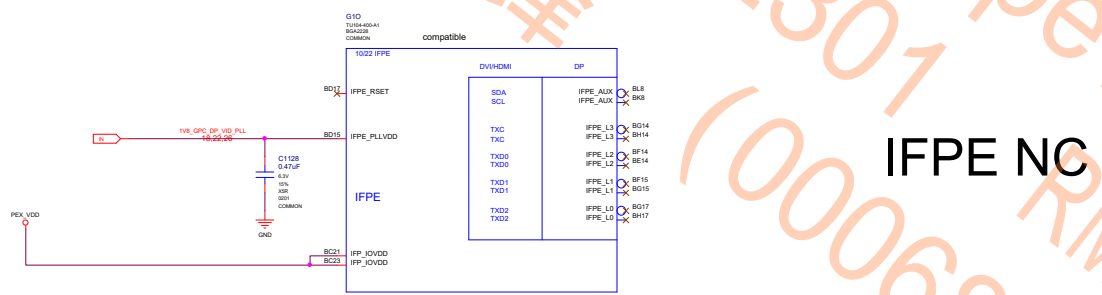
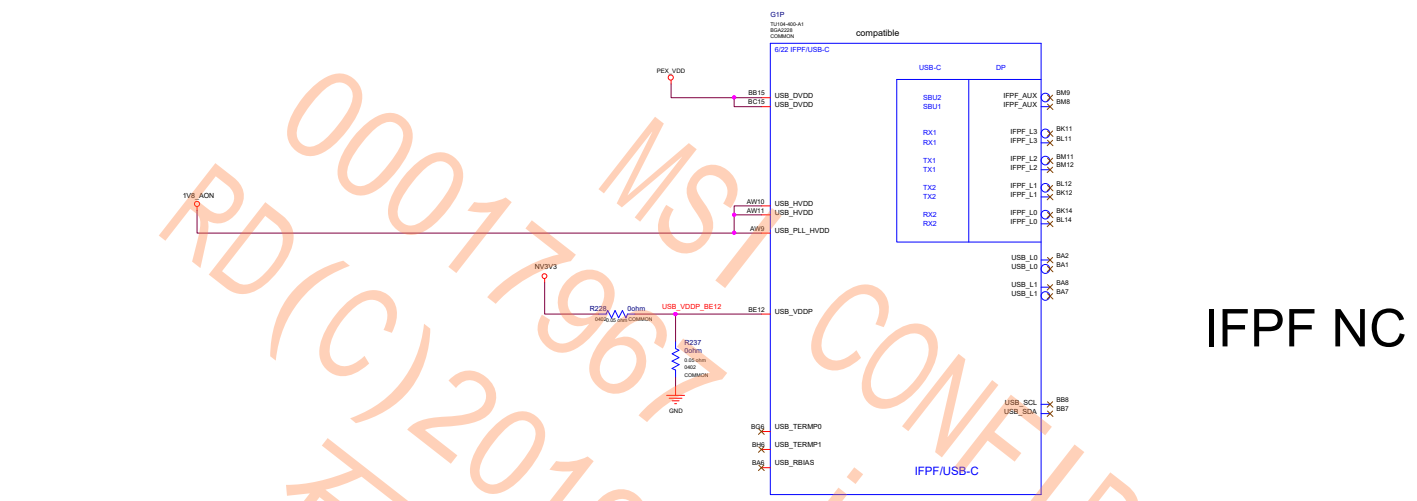


## IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL



19ci203

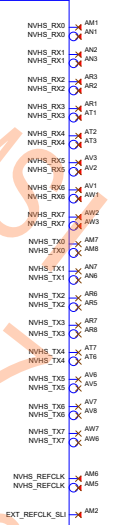














STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1.ENABLE 0.DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

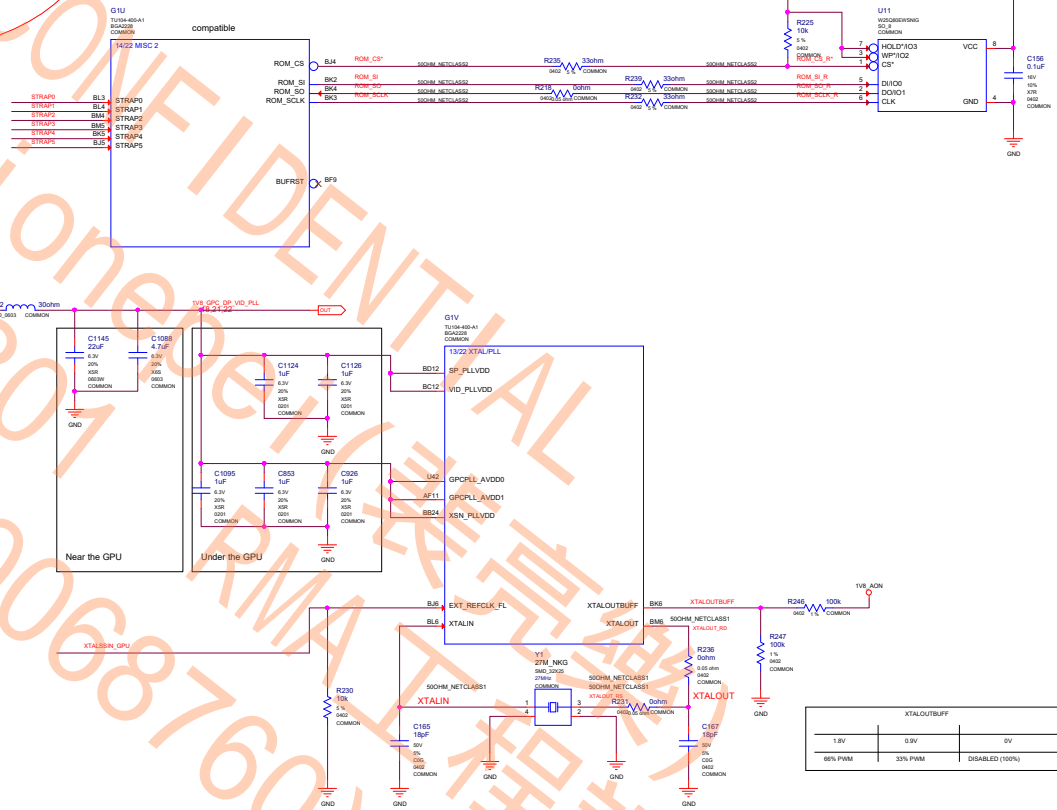
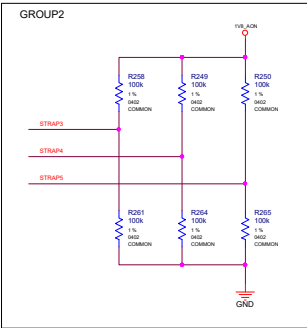
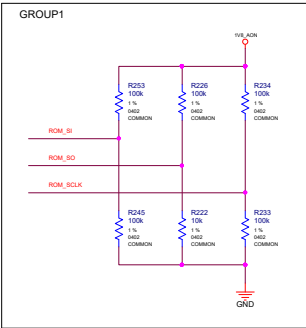
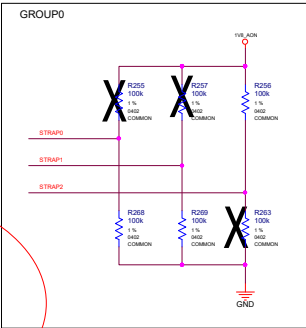
1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

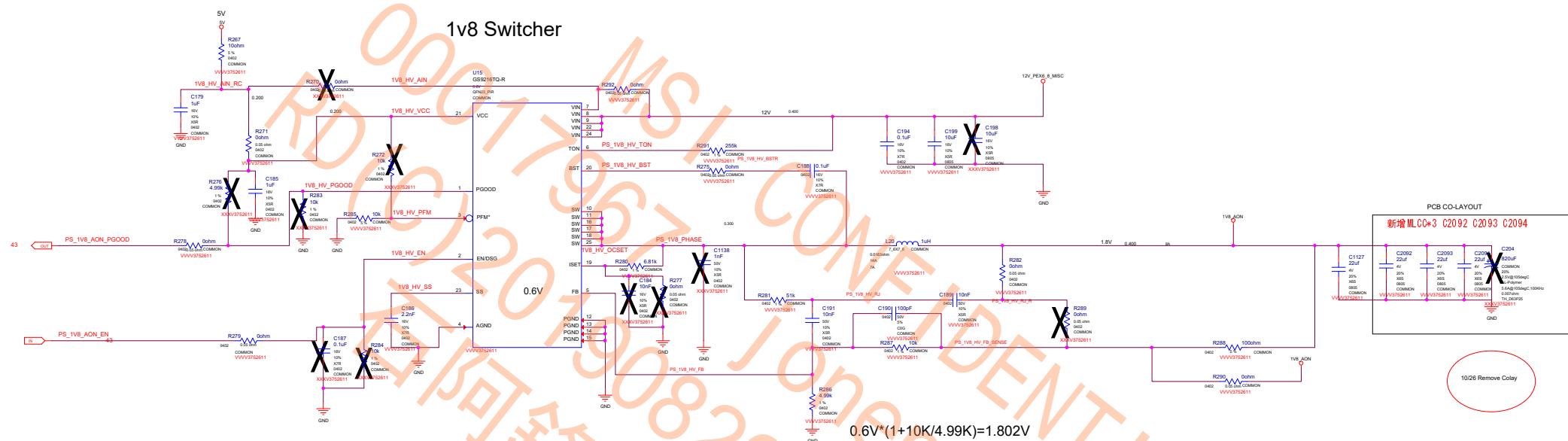
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

注意上件的MEM Straps



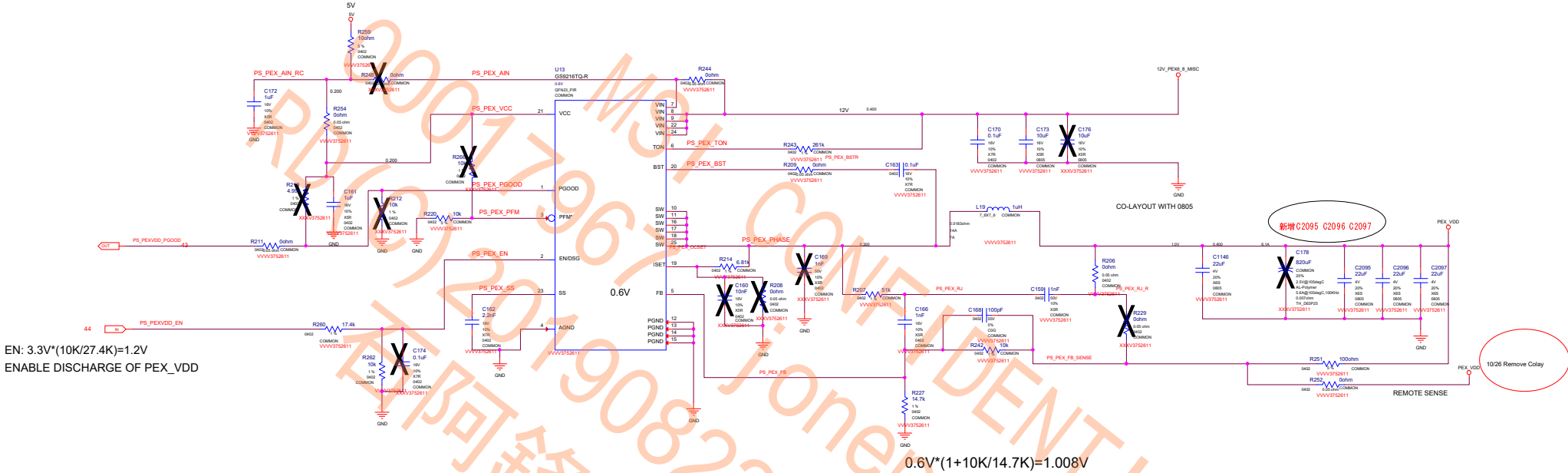
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Doc Custom	Document Description MISC2-ROM, XTAL, Straps	Rev 2.2
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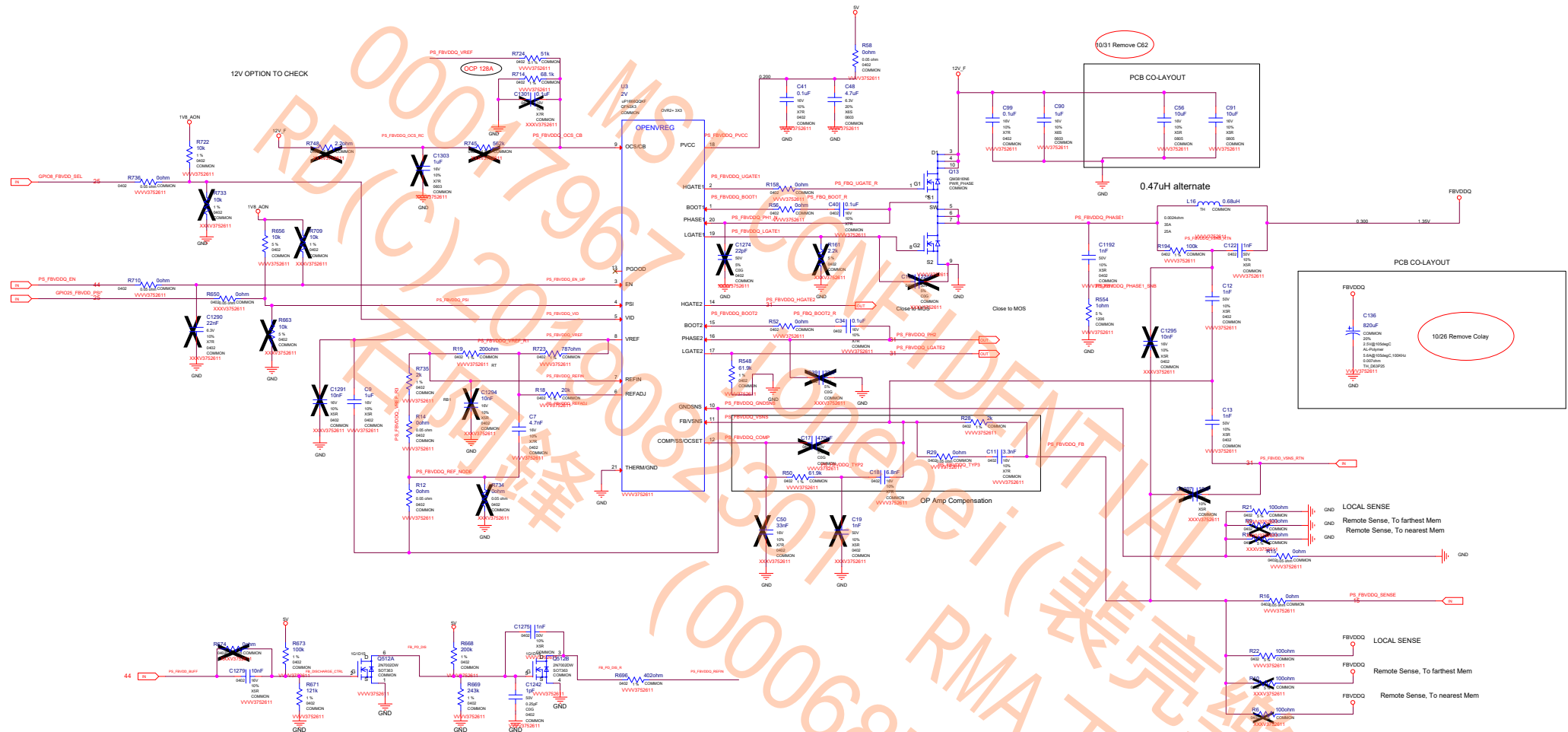


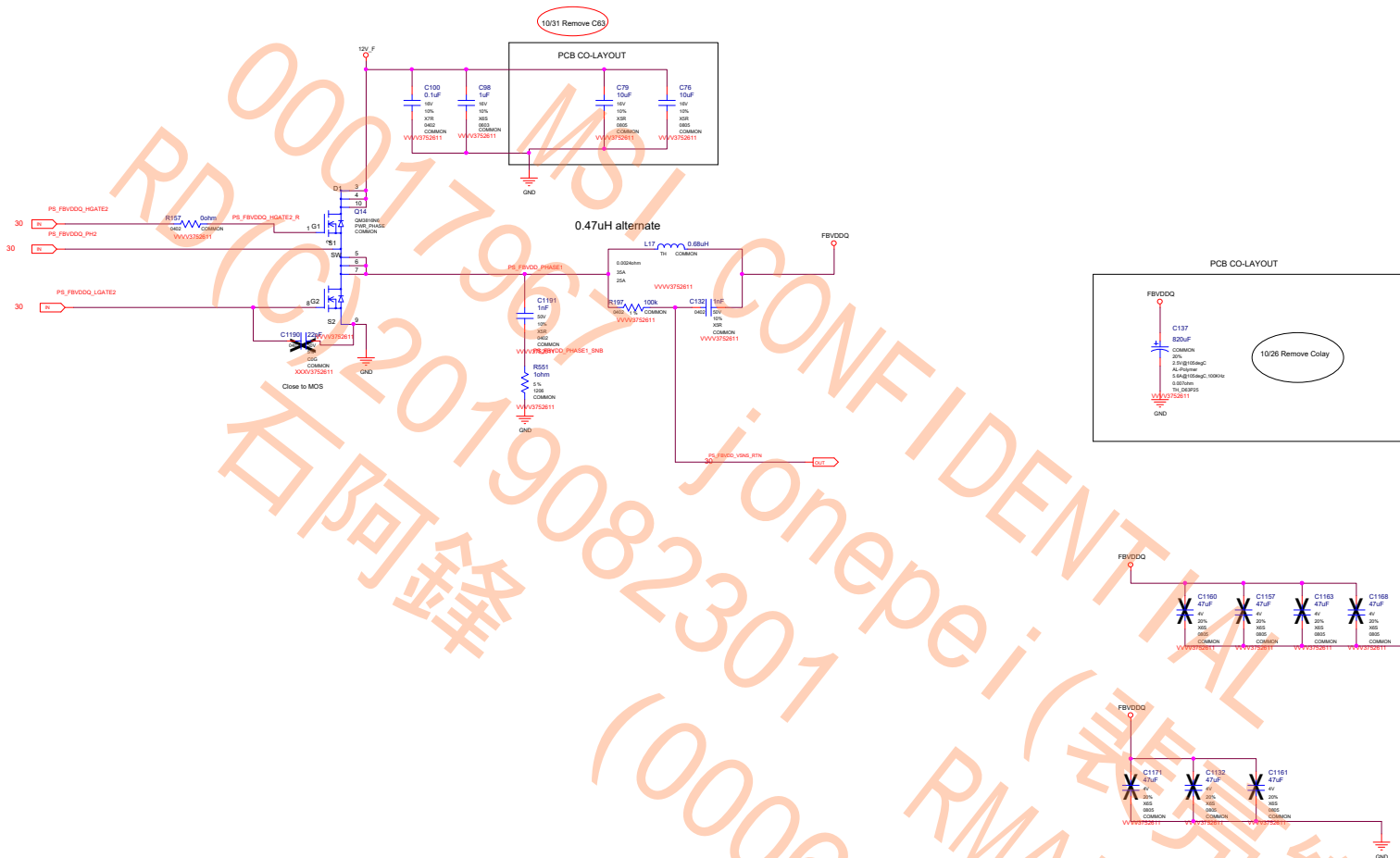


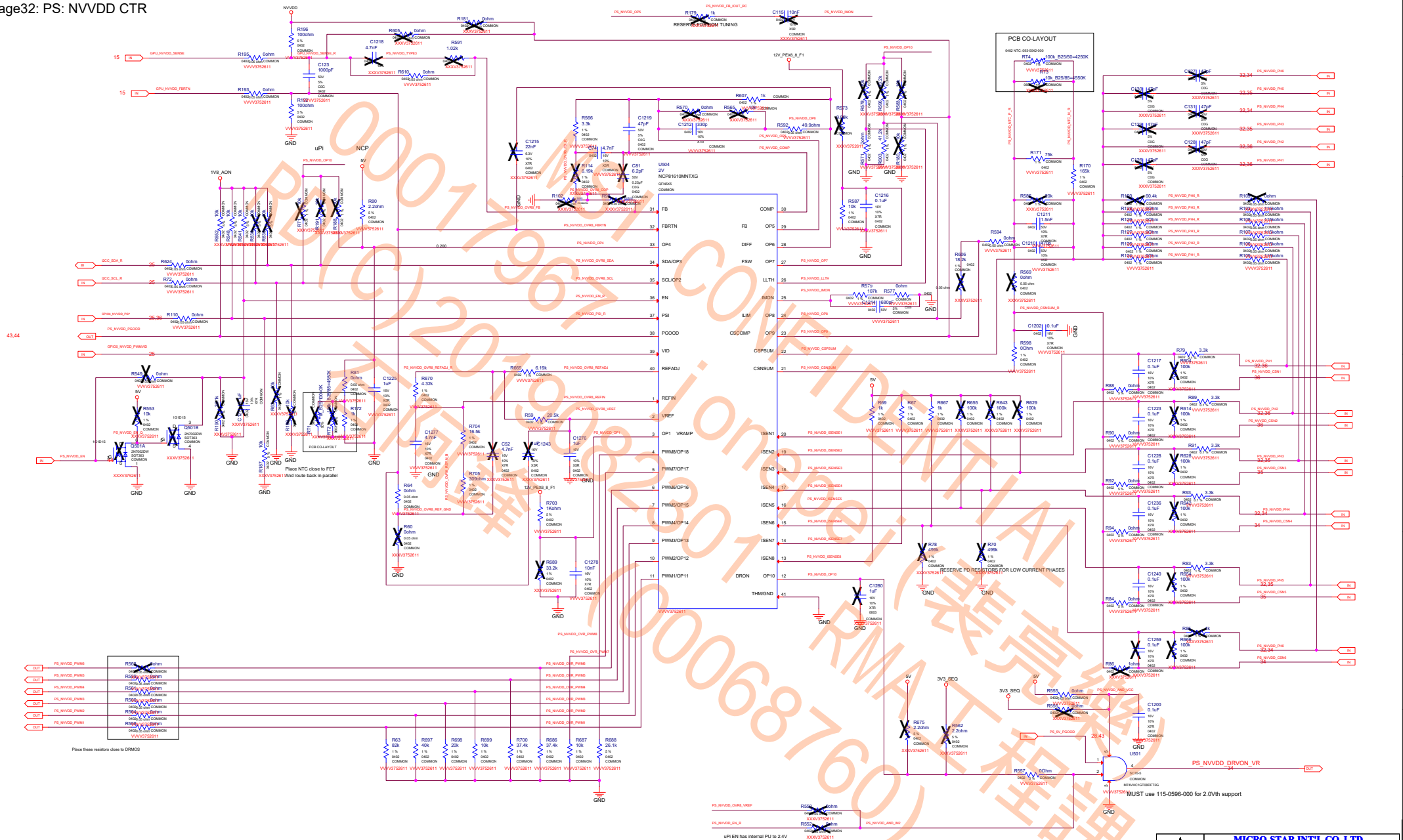
PEX Switcher







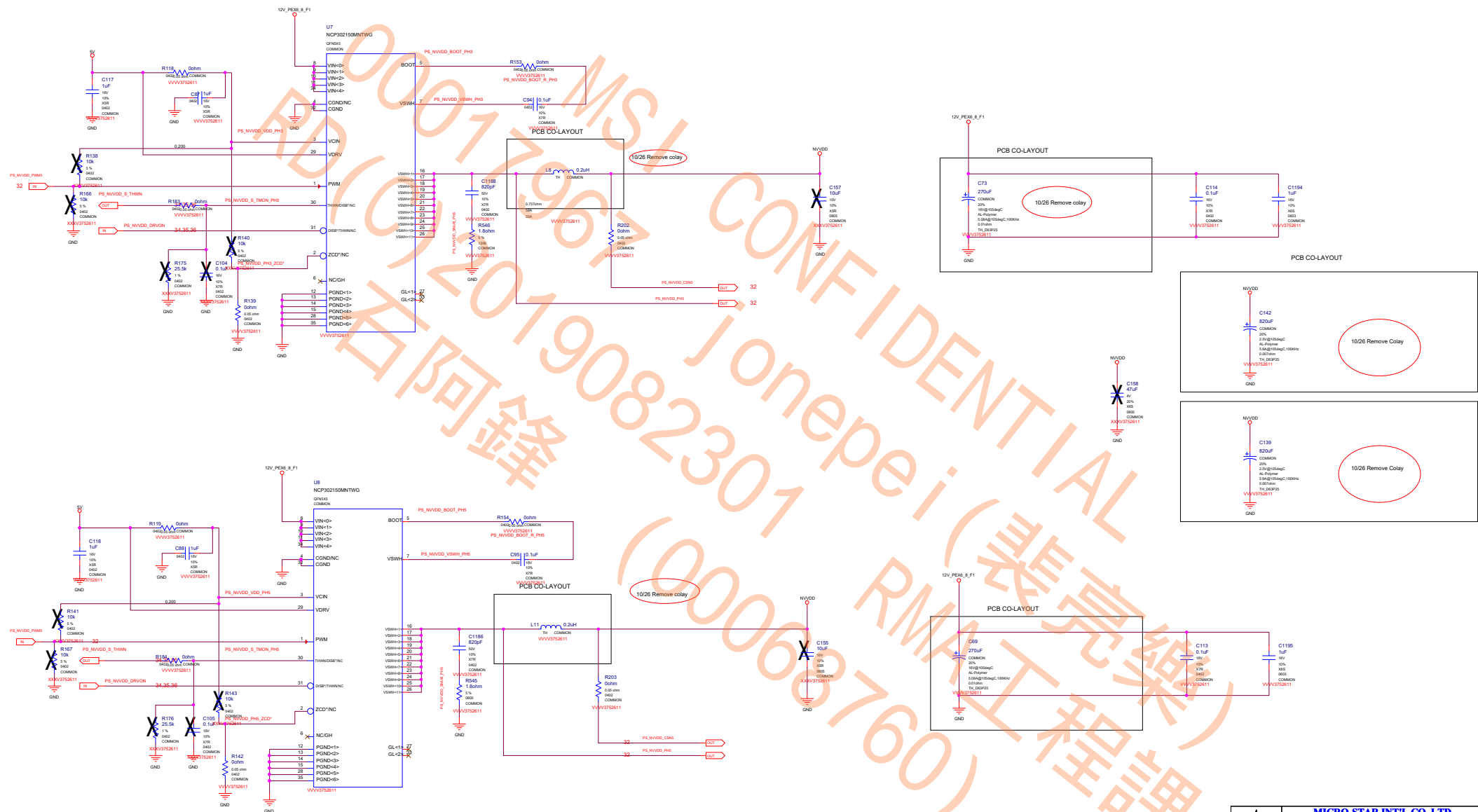


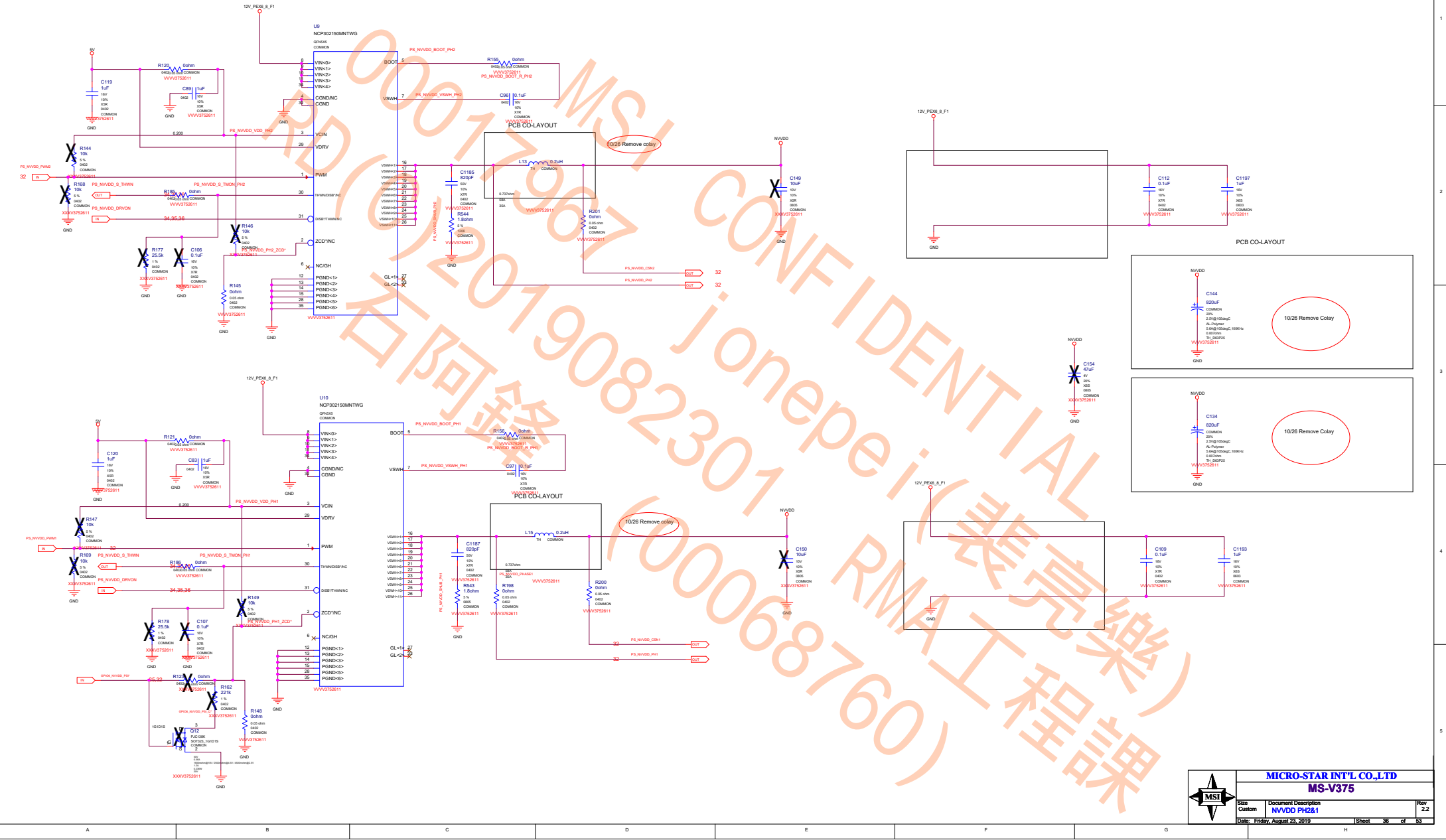


DROP OVR3i SOLUTION

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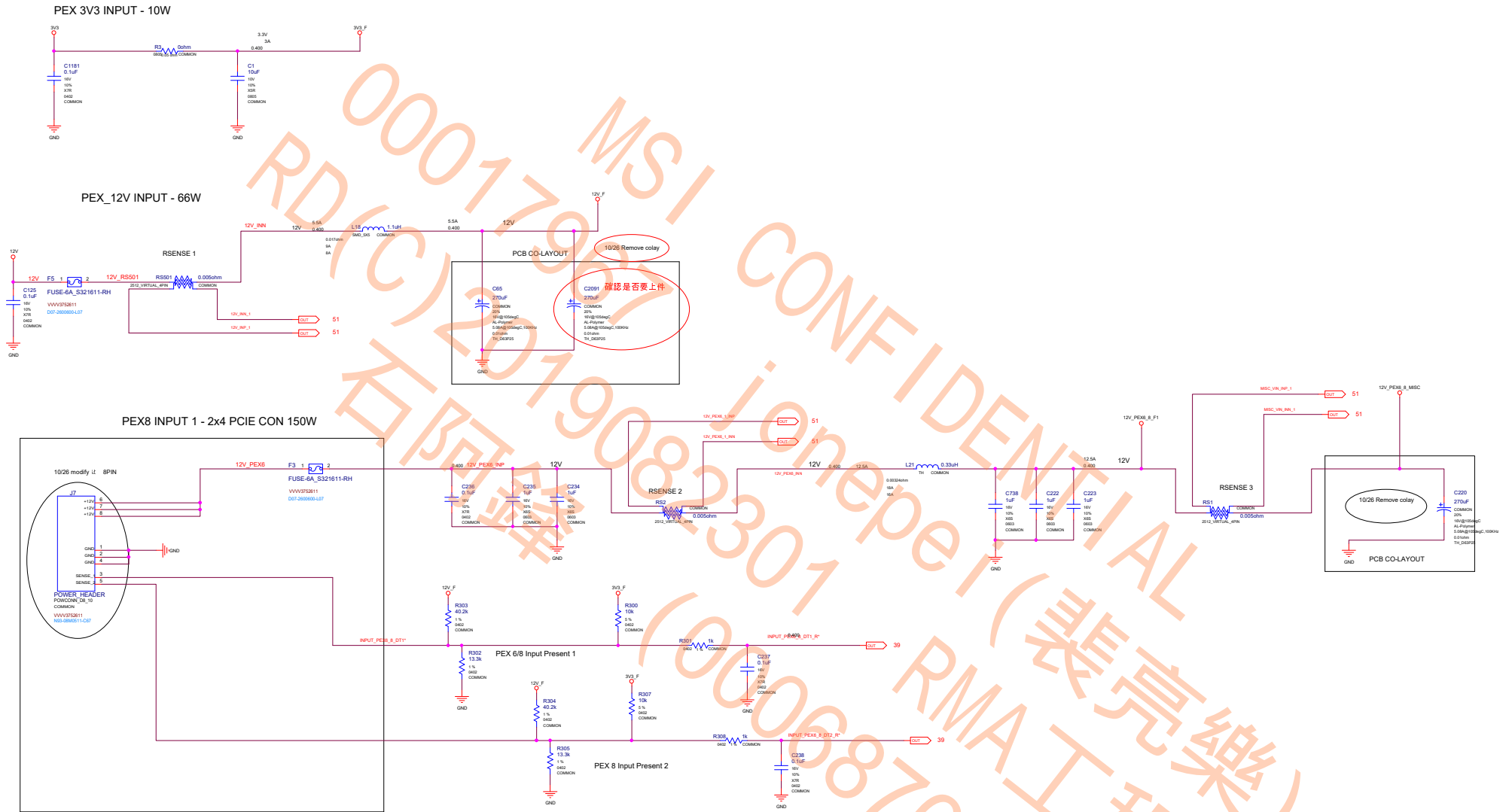


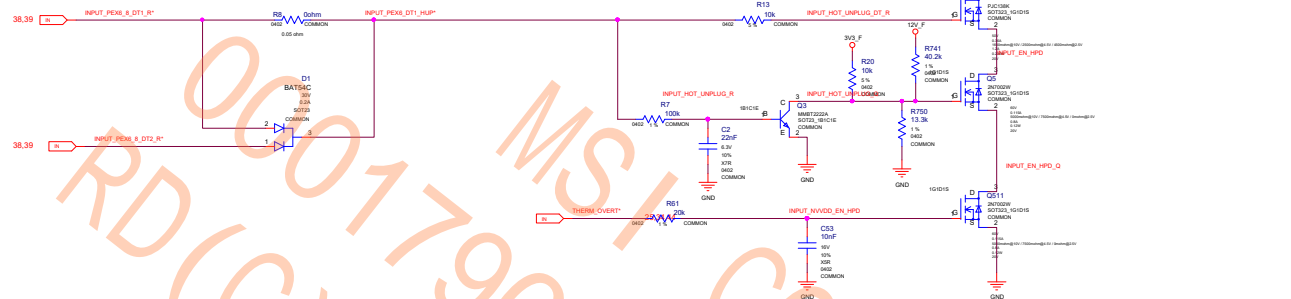




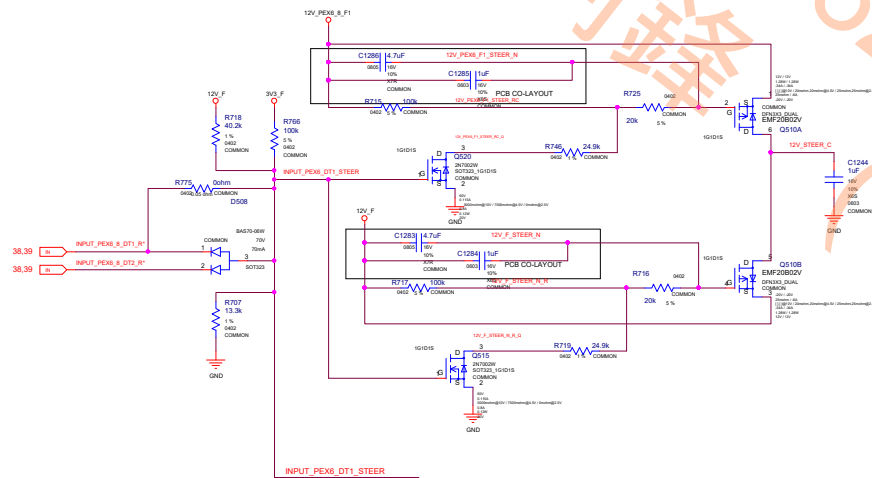
DELETE RAIL BALANCE CIRCUIT

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	Custom	Input Power Balancing Switcher	2.2
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GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA.



38.39 INPUT\_PEXB\_2\_DT1\_K

38.39 INPUT\_PEXB\_8\_DT2\_K

1V8 ACN

R1 2.2k

1.5k

GND COMMON

10101S

3 6 2

U1

10101S

3 6 2

U2


GND

GPOI2\_LOW\_PERF\*

2

GPOI2_LOW_PERF*	CPU SPEED
0	Slow
1	Normal

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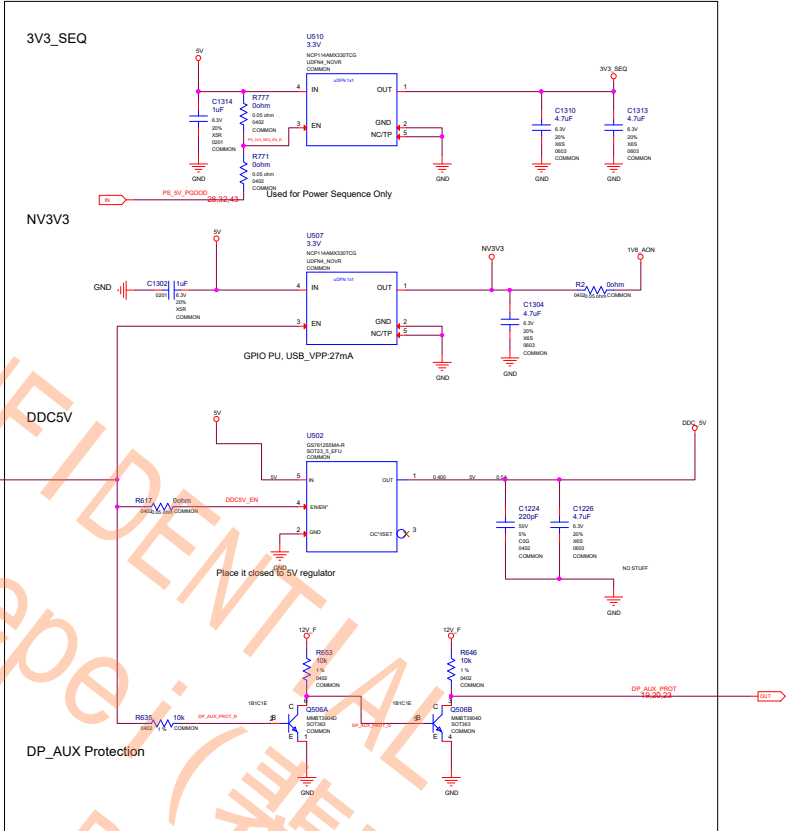
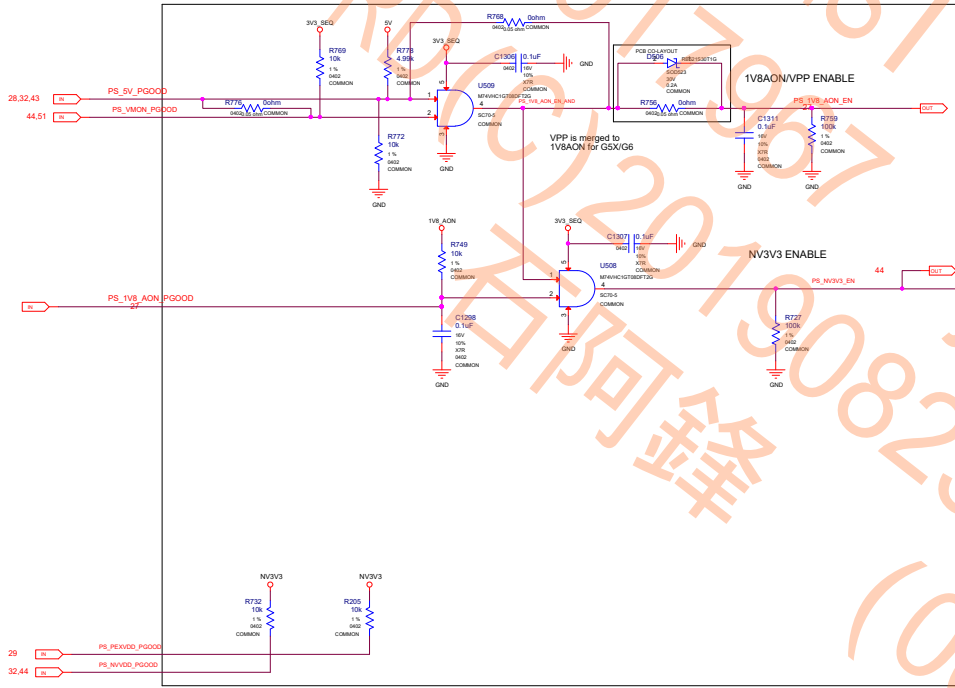
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	Custom	BUCKBOOST	2.2
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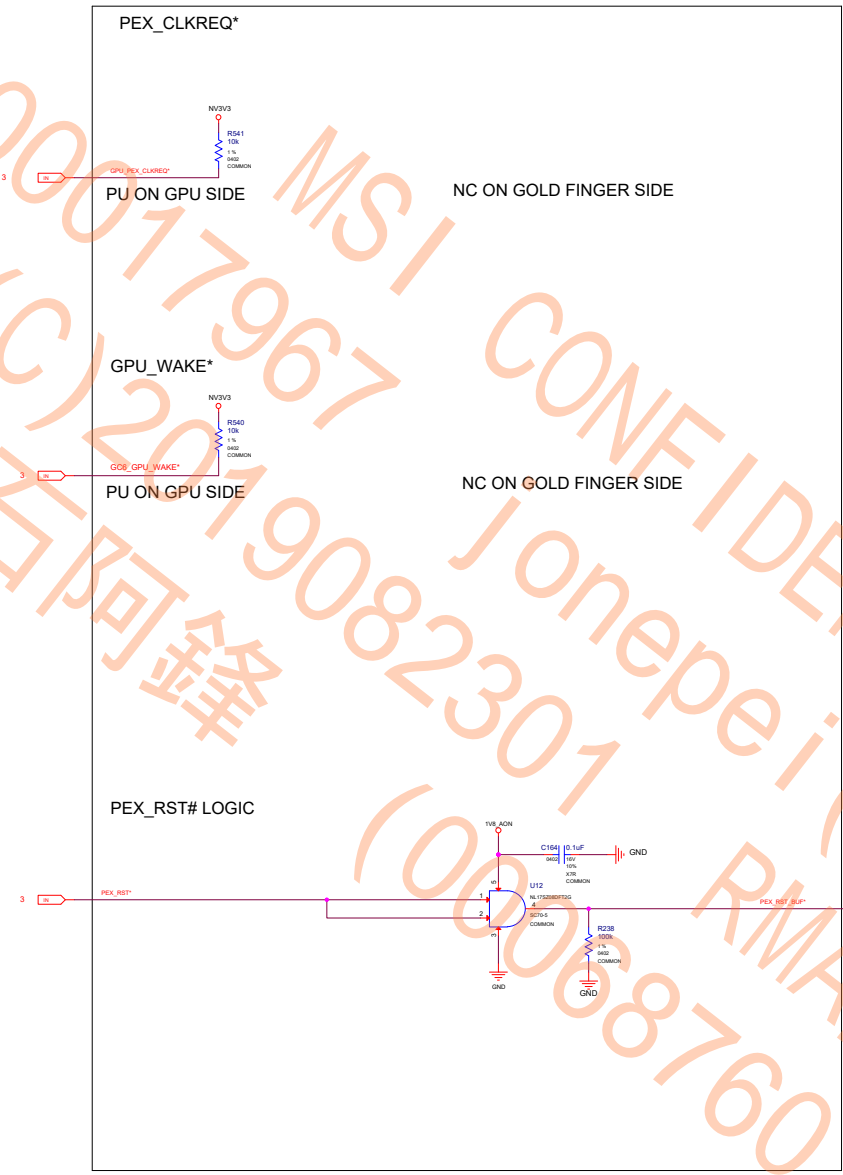


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	Custom	SEQUENCE:Voltage Monitor	2.2
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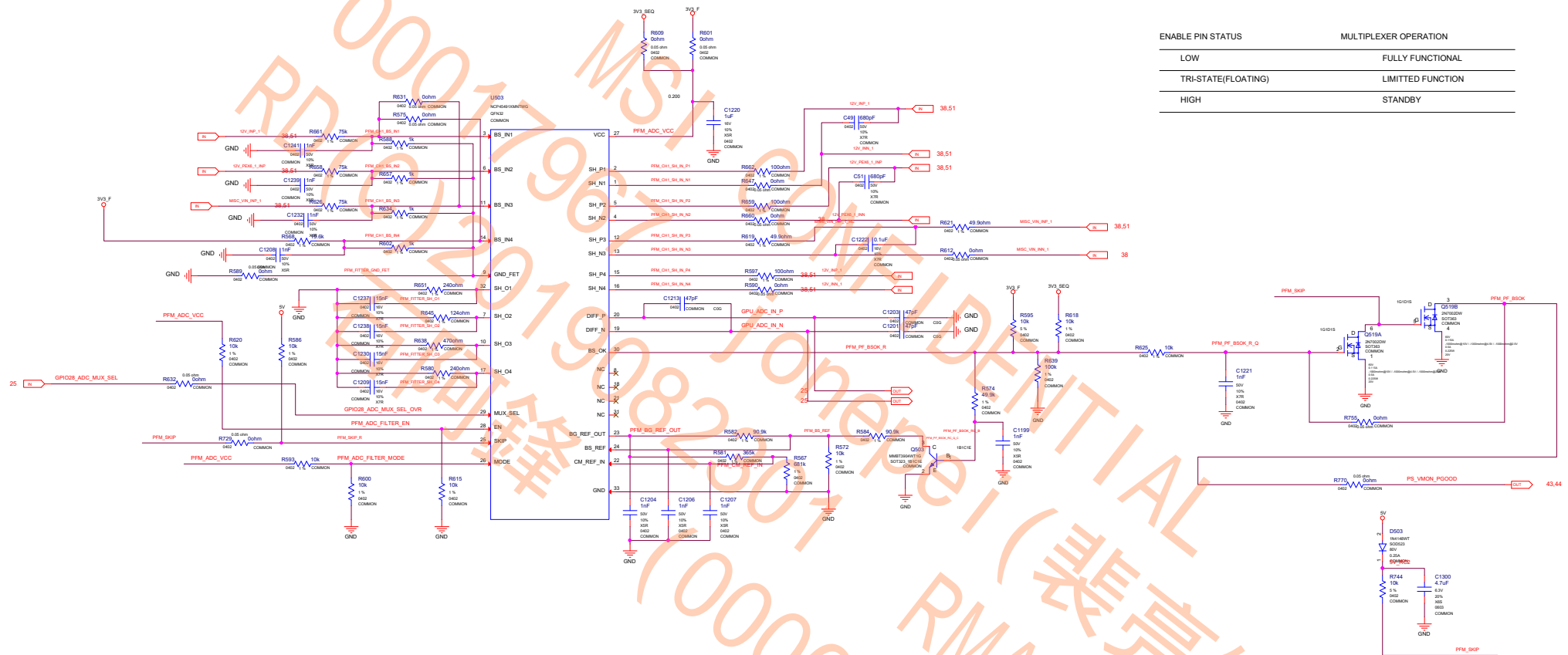


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	Custom	LOGO LED	2.2
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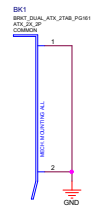




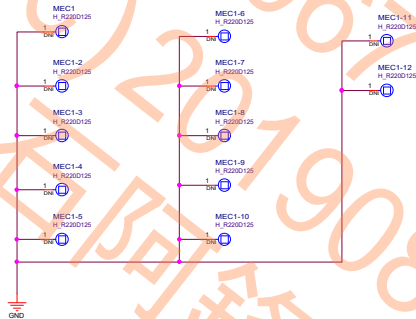
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LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

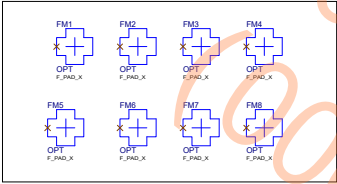
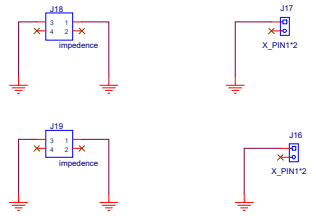
Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:





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